IN THE SPECIFICATION:

Please amend paragraph **[0002]** as follows:

[0002] The present invention relates generally to packaged semiconductor devices with a low profile. More specifically, the invention pertains to ~~wafer level~~ wafer-level packages having a true chip profile or both a chip profile and a chip footprint.

Please amend paragraph **[0003]** as follows:

[0003] The dimensions of many different types of ~~state of the art~~ state-of-the-art electronic devices are ever decreasing. To reduce the dimensions of electronic devices, the structures by which the microprocessors, memory devices, other semiconductor devices, and other electronic components of these devices are packaged and assembled with carriers, such as circuit boards, must become more compact. In general, the goal is to economically produce a chip-scale package (CSP) of the smallest size possible, and with conductive structures, such as leads, pins, or conductive bumps, which do not significantly contribute to the overall size in the X, Y, or Z dimensions, all while maintaining a very high performance level.

Please amend paragraph **[0005]** as follows:

[0005] Conventionally, semiconductor device packages are multilayered structures, typically including a bottom layer of encapsulant material, a carrier (e.g., leads, a circuit board, etc.), a semiconductor die, and a top layer of encapsulant material, for example. In addition, the leads, conductive bumps, or pins of conventional semiconductor device packages, which electrically connect such packages to carrier substrates, as well as provide support for the packages, are sometimes configured to space the semiconductor device packages apart from a carrier substrate. As a result, the overall thicknesses of these semiconductor device packages and the distances the packages protrude from carrier substrates are greater than is often desired for use in ~~state of the art~~ state-of-the-art electronic devices.

Please amend paragraph **[0006]** as follows:

[0006] ~~Wafer-level~~ Wafer-level packaging (WLP) refers to packaging of an electronic component while it is still part of a wafer. The packages that are formed by WLP processes are generally considered to be "chip-sized" packages, at least with respect to the lateral X and Y dimensions, i.e., "footprint", but typically have somewhat enlarged profiles in the Z dimension due to the solder balls, pins, or other conductive structures that protrude therefrom. Likewise, modules of stacked dice may use interdie connections comprising solder balls, pins, etc., which substantially contribute to the overall Z dimension, i.e., profile.

Please amend paragraph **[0007]** as follows:

[0007] "Flip-chip" technology, as originating with ~~controlled collapse~~ controlled-collapse chip connection (C-4) technology, is an example of an assembly and packaging technology that results in a semiconductor device being oriented substantially parallel to a carrier substrate, such as a circuit board. In flip-chip technology, the bond pads or contact pads of a semiconductor device are arranged in an array over a major surface of the semiconductor device. Flip-chip techniques are applicable to both bare and packaged semiconductor devices. A packaged flip-chip type semiconductor device, which typically has solder balls arranged in a so-called "ball grid array" (BGA) connection pattern, typically includes a semiconductor die and a carrier substrate, which is typically termed an "interposer". The interposer may be positioned adjacent either the back side of the semiconductor die or the active (front) surface thereof.

Please amend paragraph **[0008]** as follows:

[0008] When the interposer is positioned adjacent the back side of the semiconductor die, the bond pads of the semiconductor die are typically electrically connected by way of wire bonds or other intermediate conductive elements to corresponding contact areas on a top side of the interposer. These contact areas communicate with corresponding bumped contact pads on the back side of the interposer. This type of flip-chip assembly is positioned adjacent ~~a higher~~

~~level~~ higher-level carrier substrate with the back side of the interposer facing the carrier substrate.

Please amend paragraph **[0012]** as follows:

[0012] The thicknesses of conventional flip-chip type packages having ball grid array connection patterns are defined by the combined thicknesses of the semiconductor die, the interposer, the adhesive material therebetween, and the conductive structures (e.g., solder balls) that protrude above the interposer or the semiconductor die. As with the flat packages, conventional flip-chip type packages are often undesirably thick for use in small, thin, ~~state of the art~~ state-of-the-art electronic devices. Furthermore, use of this general construction method for producing a stacked multichip module (MCM) results in a relatively high-profile, large footprint device.

Please amend paragraph **[0025]** as follows:

[0025] FIG. 2 is a plan view of an enlarged portion of the exemplary fabrication substrate of FIG. 1, with multiple semiconductor devices fabricated thereon in accordance with teachings of the invention, each semiconductor device including bond pads that are arranged ~~in-line~~ in-line along a central portion of the semiconductor device, which bond pads are redistributed to outer connectors that are positioned on opposite peripheral edges thereof;

Please amend paragraph **[0038]** as follows:

[0038] Referring to FIGS. 1 and 2, a fabrication substrate, which is also referred to herein as a substrate blank 8, is shown. One side of the substrate blank 8 is selected as an active surface 18 and the opposite side becomes the back side 19. A pattern of straight boundary lines or streets 12 and 14 (individually referred to herein as streets 12A, 12B, 12C, ~~etc.~~ etc., and 14A, 14B, 14C, etc., respectively), which respectively extend in the X direction and Y direction, is delineated for subdivision of the substrate blank 8 into a plurality of areas at which separate semiconductor devices 16 are to be fabricated and further processed to form packages 10

(individually referred to as packages 10A, 10B, 10C, etc.). Streets 12 and 14 also comprise saw lines for the subsequent singulation of each package 10 from other packages 10 that have been fabricated on the substrate blank 8. For example, in FIG. 2, a package 10E is shown as being surrounded by immediately adjacent packages 10A, 10B, 10C, 10D, 10F, 10G, 10H and 10J that are carried upon the same, yet-to-be severed substrate blank 8.

Please amend paragraph **[0040]** as follows:

[0040] The fabrication of semiconductor devices 16 may be effected in accordance with the desired ~~end use~~ end use of the assembled package 10 of which each semiconductor device is intended to be a part. An integrated circuit (not shown) is formed in each semiconductor device 16 to interface with the active surface 18, as known in the art. A wide variety of integrated circuit device elements may be used in the semiconductor device 16 of a package 10, including, for example, conductors, resistors, transistors, capacitors, inductors, insulators, and the like. Fabrication processes are used which typically fall into the groups known as layering, patterning, doping and heating, and many specific variations of each are well known. For example, useful layering processes include various methods of oxidation, chemical vapor deposition (CVD), molecular beam epitaxy, physical vapor deposition (PVD), and other techniques.

Please amend paragraph **[0042]** as follows:

[0042] In addition to a semiconductor device 16 (FIG. 1), the packages 10A, 10B, 10C, 10D, 10E, etc. on the substrate blank 8 each include conductive traces 28 that extend between various bond pads 20 and, prior to severing the packages 10A, 10B, 10C, 10D, 10E, ~~etc.~~ etc., from one another, corresponding conductive vias 30, such as vias 30A, 30B, 30C, which are depicted, by way of example only, as being annular in shape. The conductive vias 30 extend completely through the thickness of the substrate blank 8 and, thus, through the entire thickness of the package 10 of which they will become a part. For each conductive via 30 that is located between adjacent, functional semiconductor devices 16, a conductive trace 28 extends from a

bond pad 20 of each of the adjacent, functional semiconductor devices 16 to that conductive via 30. Each of the conductive vias 30 is positioned along a street 12, 14 (in this example, streets 14A, 14B, 14C, etc.) on the substrate blank 8. Each conductive via 30 also extends laterally into at least a portion of the semiconductor devices 16 between which it is positioned. For example, packages 10E and 10F share conductive vias 30C on the boundary line 14C between the two packages 10E and 10F. Package 10D also shares conductive vias 30B with package 10E.

Please amend paragraph **[0045]** as follows:

[0045] FIG. 5 is a cross-sectional view of a portion of a package 10. Semiconductor device 16 of package 10 includes integrated circuits 42, although only a single integrated circuit 42 is schematically depicted in FIG. 5. Each integrated circuit 42 terminates at a bond pad 20 on the active surface 18 of the semiconductor device 16. An upper insulative layer, i.e., a dielectric layer 36, which is formed on the active surface 18, provides some protection for the underlying integrated circuit 42. Conductive traces 28 (again, only one is shown) are formed atop the dielectric layer 36 and extend from each bond pad 20 toward corresponding via through-holes 38, which are located on a street 12, 14 that defines a periphery of the semiconductor device 16. A second insulative layer, or dielectric coating 44, may be formed so as to cover at least a portion of the top 32 of package 10. The second dielectric coating 44 may be formed before or after the via through-holes 38 are formed. A conductive via 30, which includes a quantity of conductive material, such as one or more layers of metal, conductive or conductor-filled elastomer, or the like, deposited in or on the surfaces of a via through-hole 38, may be located within ~~in each~~ each via through-hole 38. An insulative lining 39 on the surfaces of each via through-hole 38 may electrically isolate each conductive via 30 from substrate blank 8. As conductive vias 30 are positioned on a street 12, 14 that is common to the package 10 and a neighboring, like package 10X on the substrate blank 8, each conductive via 30 may be temporarily shared between adjacent packages 10 and 10X. As depicted, the conductive via 30 will subsequently be severed to form two or more outer connectors 31, each of which

includes a recess 40 formed therein. The back side 19 of the semiconductor device 16 may be at least partially coated with a lower protective insulative layer 46, as known in the art.

Please amend paragraph **[0046]** as follows:

[0046] Turning now to FIGS. 6, 7, 8, and 9, various exemplary configurations of conductive traces 28, which are applied to the package tops 32 at the wafer level, are illustrated. The conductive traces 28, which may be considered to be redistribution metallization, extend generally laterally from each bond pad 20 to a desired outer connector 31 (see, e.g., FIGS. 4 and 5) location at a periphery of the package 10 and may be joined to conductive traces 28 of adjacent packages 10 at a street 12, 14 therebetween. In each of FIGS. 6-9, portions of two adjacent ~~wafer-level~~ wafer-level packages 10D and 10E are shown with an intervening street 14. In FIG. 6, the conductive traces 28 have substantially uniformly widths and extend between bond pads 20 on the two packages 10D and 10E, intersecting the street 14 between packages 10D and 10E.

Please amend paragraph **[0047]** as follows:

[0047] The conductive traces 28 may be formed by a wide range of processes known in the art. By way of example, one or more layers of conductive material, such as metal (e.g., aluminum, copper, gold, nickel, etc.), may be formed on package tops 32 by any suitable process, including, without limitation, chemical vapor deposition (CVD), physical vapor deposition (PVD) (e.g., sputtering or evaporation), electrolytic plating, electroless plating, and immersion plating techniques. While such a layer of conductive material may be formed before, simultaneously with, or following the introduction of conductive material into via ~~through-holes~~ through-holes 38 (see, e.g., FIGS. 10-13), in the embodiments that are shown in FIGS. 6-9, the layer of conductive material from which the conductive traces 28 are formed would be deposited prior to the formation of via through-holes 38 and, thus, prior to the introduction of conductive material into the via through-holes 38. Next, the layer of conductive material may be patterned, as known in the art, such as by use of mask and etch techniques.

Please amend paragraph **[0050]** as follows:

[0050] In FIGS. 8 and 12, conductive traces 28″ are shown as including ~~diamond-shaped~~ diamond-shaped enlargements 58″ at intersections 66 along a street 14 between two adjacent packages 10D, 10E. Adjacent diamond-shaped enlargements 58″ may contact one another at areas 80, which are subsequently removed when packages 10D and 10E are severed from one another, thereby electrically isolating adjacent enlargements 58″ from one another.

Please amend paragraph **[0055]** as follows:

[0055] As depicted in FIG. 14 with respect to packages 10D and 10E that are still structurally connected to one another, or at the wafer level, a conductive via 30 may be formed in a via through-hole 38 by introducing a quantity of conductive material 29 onto at least the surfaces of each via through-hole 38. The conductive material 29 contacts at least edge regions of a conductive trace 28 or enlargement 58 located adjacent to an opening of that via ~~through-hole~~ through-hole 38. While FIG. 14 depicts the conductive vias 30 as being annular in shape, the conductive vias 30 may optionally be substantially solid structures. The shapes of the conductive vias 30 may result from the methods by which conductive material 29 is introduced into the via ~~through-holes~~ through-holes 38. By way of example only, electroless deposition, immersion deposition, electrolytic deposition, chemical vapor deposition (CVD), or physical vapor deposition (PVD) (e.g., sputtering, evaporation, etc.) techniques may be employed. Alternatively, via through-holes 38 may be filled with conductive material 29 in the form of solder or another metal or metal alloy, conductive or conductor-filled elastomer, or other conductive materials which have properties that make them suitable for use as outer connectors 31 (e.g., low contact resistance with the materials of adjacent conductive structures, good adhesion to adjacent materials, etc.). Examples of conductive materials 29 that may be used to form conductive vias 30 and, thus, outer connectors 31 (FIGS. 3-5) include, but are not limited to, nickel-plated copper, aluminum, and other solder-compatible materials.

Please amend paragraph **[0057]** as follows:

[0057] Turning again to FIG. 12, it can be seen that, in singulation of packages 10D and 10E along street 14, the kerf width 74 may also remove ~~areas~~ areas 80 where enlargements 58″ of adjacent conductive traces 28″ are continuous with one another, such as the ~~corners 80~~ corners of the diamond-shaped enlargements 58″ depicted in FIG. 12, thus separating and electrically isolating adjacent conductive traces 28″ from each other. Accordingly, when the kerf width 74 is sufficient to mechanically separate adjacent enlargements 58″, a further etching step to separate the enlargements 58″ from each other is unnecessary.

Please amend paragraph **[0060]** as follows:

[0060] As depicted in FIGS. 17, 18 and 19, an exemplary multichip module 90, or semiconductor device assembly, of the present invention is shown. While the illustrated multichip module 90 includes four packages 10A-10D in stacked arrangement, multichip modules with other arrangements and with other numbers of packages 10 are also within the scope of the present invention. By way of example only, stacked multichip modules 90 that include a greater number of packages 10 would be particularly useful for ~~high capacity~~ high-capacity memory.

Please amend paragraph **[0067]** as follows:

[0067] If desired (e.g., in packages that include outer connectors 31 arranged along only one or two adjacent peripheral edges 22, 24 thereof), conductive columns 88 may be secured to their outer connectors 31. One example of the manner in which a conductive column 88 may be secured to a set of corresponding outer connectors 31 includes the use of a conductive adhesive, such as solder, another metal or metal alloy, a conductive or ~~conductor-filled~~ conductor-filled elastomer, or the like, which may be positioned between a conductive column 88 and each of its corresponding outer connectors 31, around an outer periphery of the conductive column 88 and in contact with lateral edges of each of the outer connectors 31 that corresponds thereto, or in a combination of these locations. Optionally, the conductive

columns 88 may be coated with tin to enhance connection to the outer connectors 31 in this manner. As another example, a nonconductive material may be disposed around a surface of each conductive column 88 that does not contact outer connectors 31, as well as to a peripheral edge 22, 24 of each package 10 of the multichip module 90, to maintain contact and, thus, an electrical connection between each conductive column 88 and its corresponding outer connectors 31.

Please amend paragraph **[0069]** as follows:

[0069] Following assembly of the ~~supporting~~ support substrate 82 with all the packages 10 in the stack and the establishment of contact between conductive columns 88 and corresponding sets of outer connectors 31, the conductive columns 88 may be cut, or trimmed, to remove any excess portion extending beyond the uppermost package 10. The conductive columns 88 may alternatively be provided with a length that corresponds to the height at which packages 10 are to be stacked in the multichip module 90.